WHAT IS CLAIMED IS:

1. An in-service programmable logic array, comprising:

a first logic plane that receives a number of input signals, the first logic plane having a plurality of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs;

a second logic plane having a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the in service programmable logic array implements a logical function; and

wherein each of the logic cells includes a floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

2. The in-service programmable logic array of claim 1, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

3. The in-service programmable logic array of claim 1, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

4. The in-service programmable logic array of claim 3, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. The in-service programmable logic array of claim 1, whereing the low tunnel barrier intergate insulator includes a Perovskite oxide tunnel barrier.

6. The in-service programmable logic array of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

7. The in-service programmable logic array of claim 6, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

8. The in service programmable logic array of claim 1, wherein the first logic plane and the second logic plane each comprise NOR planes.

9. A programmable logic array, comprising:

a plurality of input lines for receiving an input signal;

a plurality of output lines; and

one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein the first logic plane and the second logic plane comprise a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to a received input signal, wherein each logic cell includes a vertical non-volatile memory cell including:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

10. The programmable logic array of claim 9, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

11. The programmable logic array of claim 9, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

12. The programmable logic array of claim 11, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

13. The programmable logic array of claim 9, wherein the floating gate includes a vertical floating gate formed alongside of the body region.

14. The programmable logic array of claim 13, wherein the control gate includes a vertical control gate formed alongside of the vertical floating gate.

15. The programmable logic array of claim 9, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

16. The programmable logic array of claim 15, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

17. A programmable logic array, comprising:

a plurality of input lines for receiving an input signal;

a plurality of output lines; and

one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein the first logic plane and the second logic plane comprise a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to a received input signal, wherein each logic cell includes a non-volatile memory cell including:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed on the metal layer;

a second metal layer formed on the metal oxide intergate insulator; and

a polysilicon control gate formed on the second metal layer.

18. The programmable logic array of claim 17, wherein first and the second metal layers are lead and the metal oxide intergate insulator is lead oxide (PbO).

19. The programmable logic array of claim 17, wherein the first and second metal layer are aluminum and the metal oxide intergate insulator is aluminum oxide (Al_2O_3).

20. The programmable logic array of claim 17, wherein the first and the second metal layers include transition metal layers and the metal oxide intergate insulator includes a transition metal oxide intergate insulator.

21. The programmable logic array of claim 20, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

22. The programmable logic array of claim 17, wherein the metal oxide intergate insulator includes a Perovskite oxide intergate insulator.

23. The programmable logic array of claim 17, wherein the floating gate transistor includes a vertical floating gate transistor.

24. The programmable logic array of claim 17, wherein each input line is integrally formed with the polysilicon control gate for addressing the floating gate.

25. The programmable logic array of claim 17, wherein each input line is integrally formed with the polysilicon control gate in a trench opposing the floating gate.

26. The programmable logic array of claim 17, wherein the programmable logic array includes a number of buried source lines which are formed integrally with the first source/drain region and are separated from the semiconductor substrate by an oxide layer.

27. The programmable logic array of claim 17, wherein each input line includes a vertically oriented input line having a vertical length of less than 100 nanometers.

28. A programmable logic array, comprising:

a plurality of input lines for receiving an input signal;

a plurality of output lines; and

one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein the first logic plane and the second logic plane comprise a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal, wherein each logic cell includes a vertical non-volatile memory cell including:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a plurality of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain region of pillars in the array; and

wherein each of the number of input lines is disposed between rows of the pillars and integrally formed with the number of control gates and opposing the floating gates of the vertical non-volatile memory cells for serving as a control gate and are separated from the number of floating gates by a low tunnel barrier integrate insulator.

29. The programmable logic array of claim 28, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

30. The programmable logic array of claim 28, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

31. The programmable logic array of claim 28, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

32. The programmable logic array of claim 28, wherein the number of floating gates includes vertical floating gates formed alongside of the body region.

33. The programmable logic array of claim 32, wherein the number of control gates includes vertical control gates formed alongside of the vertical floating gates.

34. The programmable logic array of claim 28, wherein the number of floating gates includes horizontally oriented floating gates formed alongside of the body regions.

35. The programmable logic array of claim 28, wherein the number of buried source lines are formed integrally with the first source/drain regions and are separated from the substrate by an oxide layer.

36. A low voltage programmable logic array, comprising:

a number of input lines for receiving an input signal;

a number of output lines; and

a first logic plane that receives a number of input signals on the number of input lines, the first logic plane having a number of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs;

a second logic plane coupled to the first logic plane by a number of interconnect lines, the second logic plane having a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane on the interconnect lines and that are interconnected to produce a number of logical outputs on the output lines such that the programmable logic array implements a logical function;

wherein each logic cell includes a vertical non-volatile memory cell including:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates, wherein the number of control gates are separated from the number of floating gates by a low tunnel barrier integrate insulator;

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

37. The low voltage programmable logic array of claim 36, wherein the number of input lines are disposed in a trench between rows of the pillars in the first logic plane and oppose the floating gates of the vertical non-volatile memory cells for serving as control gates, and wherein the number of interconnect lines couple to the second source/drain region in columns of pillars for implementing a logic function in the first logic plane.

38. The low voltage programmable logic array of claim 36, wherein the number of interconnect lines are disposed in a trench between rows of the pillars in the second logic plane and oppose the floating gates of the vertical non-volatile memory cells for serving as control gates, and wherein the number of output lines couple to the second source/drain region in columns of pillars for implementing a logic function in the second logic plane.

39. The low voltage programmable logic array of claim36, wherein column adjacent pillars are separated by a trench and each trench includes a pair of floating gates opposing the body regions on opposite sides of the trench.

40. The low voltage programmable logic array of claim 39, wherein each trench in the first logic plane includes a single vertically oriented input line formed between the pair of floating gates for serving as a shared control gate.

41. The low voltage programmable logic array of claim 39, wherein each trench in the second logic plane includes a single vertically oriented interconnect line formed between the pair of floating gates for serving as a shared control gate in the second logic plane.

42. The low voltage programmable logic array of claim 39, wherein each trench in the first logic plane includes a pair of vertically oriented input lines formed between the pair of floating gates, and wherein each one of the pair of vertically oriented input lines independently addresses the floating gates on opposing sides of the trench, and wherein the pair of vertically oriented input lines are separated by an insulator layer.

43. The low voltage programmable logic array of claim 39, wherein the number of input lines are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single input line in the first logic plane.

44. The low voltage programmable logic array of claim 39, wherein the number of input lines are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of input lines in the first logic plane.

45. The low voltage programmable logic array of claim 39, wherein a pair of input lines are formed above the pair of floating gates in each trench in the first logic plane for serving as control lines, and wherein the interconnect lines are coupled to the second source/drain regions in the first logic plane and are formed above the pair of floating gates in each trench in the second logic plane for serving as control lines.

46. The low voltage programmable logic array of claim 36, wherein column adjacent pillars are separated by a trench and each trench includes a horizontally oriented floating gate formed below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in column adjacent pillars on

opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body regions of the pillars.

47. The low voltage programmable logic array of claim 46, wherein the number of input lines are disposed vertically above the floating gates in the first logic plane.

48. An electronic system, comprising:

a memory;

a processor coupled to the memory; and

wherein the processor includes at least one in service programmable logic array including:

a first logic plane that receives a number of input signals, the first logic plane having a plurality of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs;

a second logic plane having a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function; and

wherein each of the logic cells includes a non-volatile memory cell including;

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator.

49. The electronic system of claim 48, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

50. The electronic system of claim 48, wherein the low tunnel barrier intergate insulator includes a transition metal oxide.

51. The electronic system of claim 50, wherein the transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

52. The electronic system of claim 48, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

53. The electronic system of claim 52, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

54. The electronic system of claim 48, wherein the first logic plane and the second logic plane each comprise NOR planes.

55. An electronic system, comprising:

a memory;

a processor coupled to the memory; and

wherein at least one of the processor and memory include an in-service programmable logic array including:

a number of input lines for receiving an input signal;

a number of output lines;

a first logic plane that receives a number of input signals on the number of input lines, the first logic plane having a number of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs;

a second logic plane coupled to the first logic plane by a number of interconnect lines, the second logic plane having a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane on the interconnect lines and that are interconnected to produce a number of logical outputs on the output lines such that the programmable logic array implements a logical function;

wherein each logic cell includes a vertical non-volatile memory cell including:

a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates, wherein the number of control gates are separated from the number of floating gates by a low tunnel barrier integrate insulator;

a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

56. The electronic system of claim 55, wherein the low tunnel barrier intergate insulator includes a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

57. The electronic system of claim 55, wherein each floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

58. The electronic system of claim 57, wherein each control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

59. The electronic system of claim 55, wherein each floating gate is a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

60. The electronic system of claim 59, wherein the number of control gates are formed in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

61. The electronic system of claim 59, wherein the number of control gates are formed in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of control gate lines each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gate lines are separated by an insulator layer.

62. The electronic system of claim 59, wherein the number of control gates are disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

63. The electronic system of claim 59, wherein the number of control gates are disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

64. The electronic system of claim 55, wherein each floating gate is a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

65. The electronic system of claim 64, wherein the number of control gates are disposed vertically above the floating gates.

66. A method for forming a programmable logic array, comprising:

forming a first logic plane that receives a number of input signals, wherein forming the first logic plane includes forming a number of logic cells arranged in rows and columns that are interconnected to provide a number of logical outputs;

forming a second logic plane, wherein forming the second logic plane includes forming a number of logic cells arranged in rows and columns that receive the outputs of the first logic plane and that are interconnected to produce a number of logical outputs such that the programmable logic array implements a logical function; and

wherein forming each of the logic cells includes;

forming a first source/drain region and a second source/drain region separated by a channel region in a substrate;

forming a floating gate opposing the channel region and separated therefrom by a gate oxide;

forming a control gate opposing the floating gate; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate.

67. The method of claim 66, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of lead oxide (PbO) and aluminum oxide (Al_2O_3).

68. The method of claim 66, wherein forming the low tunnel barrier intergate insulator includes forming a transition metal oxide insulator.

69. The method of claim 68, wherein forming the transition metal oxide insulator includes forming the transition metal oxide insulator selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

70. The method of claim 66, wherein forming the floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

71. The method of claim 70, wherein forming the control gate includes a forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

72. The method of claim 66, wherein forming the first logic plane and the second logic plane each comprise forming NOR planes.

73. A method for forming an in service programmable logic array, comprising:

forming a plurality of input lines for receiving an input signal;

forming a plurality of output lines; and

forming one or more arrays having a first logic plane and a second logic plane connected between the input lines and the output lines, wherein forming the first logic plane and the second logic plane forming a plurality of logic cells arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal, wherein forming each logic cell includes forming a vertical non-volatile memory cell including:

forming a vertical pillar extending outwardly from a semiconductor substrate at intersections of the input lines and interconnect lines and at the intersections of the interconnect lines and the output lines, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

forming a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

forming a number of control gates opposing the floating gates; and

forming a low tunnel barrier intergate insulator to separate the control gate from the floating gate

forming a number of buried source lines formed of single crystalline semiconductor material and disposed below the pillars in the array for interconnecting with the first source/drain regions of column adjacent pillars in the array.

74. The electronic system of claim 73, wherein forming the low tunnel barrier intergate insulator includes forming a metal oxide insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

75. The electronic system of claim 73, wherein forming each floating gate includes forming a polysilicon floating gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

76. The electronic system of claim 73, wherein forming each control gate includes forming a polysilicon control gate having a metal layer formed thereon in contact with the low tunnel barrier intergate insulator.

77. The electronic system of claim 73, wherein forming each floating gate includes forming a vertical floating gate formed in a trench below a top surface of each pillar such that each trench houses a pair of floating gates opposing the body regions in adjacent pillars on opposing sides of the trench.

78. The electronic system of claim 77, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates, wherein each pair of floating gates shares a single control gate line, and wherein each floating gate includes a vertically oriented floating gate having a vertical length of less than 100 nanometers.

79. The electronic system of claim 77, wherein forming the number of control gates includes forming the control gates in the trench below the top surface of the pillar and between the pair of floating gates such that each trench houses a pair of

control gates each addressing the floating gates one on opposing sides of the trench respectively, and wherein the pair of control gates are separated by an insulator layer.

80. The electronic system of claim 77, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each pair of floating gates shares a single control gate.

81. The electronic system of claim 77, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates, and wherein each one of the pair of floating gates is addressed by an independent one of the number of control gates.

82. The electronic system of claim 73, wherein forming each floating gate includes forming a horizontally oriented floating gate formed in a trench below a top surface of each pillar such that each trench houses a floating gate opposing the body regions in adjacent pillars on opposing sides of the trench, and wherein each horizontally oriented floating gate has a vertical length of less than 100 nanometers opposing the body region of the pillars.

83. The electronic system of claim 82, wherein forming the number of control gates includes forming the control gates disposed vertically above the floating gates.

84. A method for operating an in-server programmable logic array, comprising:

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection, the one or more arrays having a first logic plane and a second logic plane connected between a number of input lines and a number of output lines, wherein number of non-volatile

memory cells in the first logic plane and the second logic plane are arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal on the input lines, wherein each non–volatile memory cell includes:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a low tunnel barrier intergate insulator;

erasing charge from one or more floating gates by tunneling electrons off of the floating gate and onto the control gate.

85. The method of claim 84, wherein erasing charge from one or more floating gates by tunneling electrons off of the floating gates and onto the control gates further includes:

providing a negative voltage to the substrate of an addressed cell; and

providing a large positive voltage to the control gate of the addressed cell.

86. The method of claim 84, wherein the method further includes writing to one or more floating gates by tunneling electrons from the control gate to the floating gate in one or more addressed cells.

87. The method of claim 86, wherein writing to one or more floating gates by tunneling electrons from the control gate to the floating gate in one or more addressed cells further includes:

applying a positive voltage to the substrate of an addressed cell; and

applying a large negative voltage to the control gate of the addressed cell.

88. The method of claim 84, wherein erasing charge from the floating gate by tunneling electrons off of the floating gate and onto the control gate includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator.

89. The method of claim 88, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator selected from the group consisting of PbO, Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

90. The method of claim 88, wherein tunneling electrons from the floating gate to the control gate through a low tunnel barrier intergate insulator includes tunneling electrons from a metal layer formed on the floating gate in contact with the low tunnel barrier intergate insulator to a metal layer formed on the control gate and also in contact with the low tunnel barrier intergate insulator.

91. A method for operating an in-server programmable logic array, comprising:

writing to one or more floating gates of a number of non-volatile memory cells in one or more arrays using channel hot electron injection, the one or more arrays having a first logic plane and a second logic plane connected between a number of input lines and a number of output lines, wherein number of non-volatile

memory cells in the first logic plane and the second logic plane are arranged in rows and columns for providing a sum-of-products term on the output lines responsive to the received input signal on the input lines, wherein each non–volatile memory cell includes:

a number of pillars extending outwardly from a substrate, wherein each pillar includes a first source/drain region, a body region, and a second source/drain region;

a number of floating gates opposing the body regions in the number of pillars and separated therefrom by a gate oxide;

a number of control gates opposing the floating gates;

a number of buried sourcelines disposed below the number of pillars and coupled to the first source/drain regions along a first selected direction in the array of non–volatile memory cells;

a number of control gate lines formed integrally with the number of control gates along a second selected direction in the array of non–volatile memory cells, wherein the number of control gates lines are separated from the floating gates by a low tunnel barrier intergate insulator; and

a number of bitlines coupled to the second source/drain regions along a third selected direction in the array of non–volatile memory cells; and

erasing charge from the one or more floating gates by tunneling electrons off of the one or more floating gates and onto the number of control gates.

92. The method of claim 91, wherein erasing charge from the one or more floating gates by tunneling electrons off of the floating gate and onto the number of control gate further includes:

providing a negative voltage to a substrate of one or more non-volatile memory cells; and

providing a large positive voltage to the control gate for the one or more non-volatile memory cells.

93. The method of claim 92, wherein the method further includes erasing an entire row of non-volatile memory cells by providing a negative voltage to all of the substrates along an entire row of non-volatile memory cells and providing a large positive voltage to all of the control gates along the entire row of non-volatile memory cells.

94. The method of claim 92, wherein the method further includes erasing an entire block of non-volatile memory cells by providing a negative voltage to all of the substrates along multiple rows of non-volatile memory cells and providing a large positive voltage to all of the control gates along the multiple rows of non-volatile memory cells.